MSLIN-98-002CCC_CIPB

March 19, 2004

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: Serial No. 10/783,195 02/20/04

M.S. Lin et al.

TOP LAYERS OF METAL FOR HIGH PERFORMANCE IC'S

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on March 25, 2004.

Stephen B. Ackerman, Reg.# 37761

Signature/Date 3/25/04

U.S. Patent 5,212,403 to Nakanishi et al., "Integrated Circuit Device having an IC Chip Mounted on the Wiring Substrate and having Suitable Mutual Connections Between Internal Circuits", shows a method of forming wiring connections both inside and outside (in a wiring substrate over the chip) for a logic circuit depending on the length of the wire connections.

U.S. Patent 5,501,006 to Gehman, Jr. et al., "Method for Connection of Signals to an Integrated Circuit", shows a structure with an insulating layer between the integrated circuit (IC) and the wiring substrate. A distribution lead connects the bonding pads of the IC to the bonding pads of the substrate.

U.S. Patent 5,055,907 to Jacobs, "Extended Integration Semiconductor Structure with Wiring Layers", discloses an extended integration semiconductor structure that allows manufacturers to integrate circuitry beyond the chip boundaries by forming a thin film multi-layer wiring decal on the support substrate and over the chip.

U.S. Patent 5,635,767 to Wenzel et al., "Semiconductor Device having Built-In High Frequency Bypass Capacitor", teaches a method for reducing RC delay by a PBGA that separates multiple metal layers.

U.S. Patent 5,106,461 to Volfson et al., "High-Density, Multi-Level Interconnects, Flex Circuits, and Tape for TAB", teaches a multi-layer interconnect structure of alternating polyimide (dielectric) and metal layers over an IC in a TAB structure.

U.S. Patent 5,686,764 to Fulcher, "Flip Chip Package with Reduced Number of Package Layers", shows a flip chip substrate that reduces RC delay by separating the power and I/O traces.

U.S. Patent 5,083,187 to Lamson et al., "Integrated Circuit Device having Bumped Power Supply Buses Over Active Surface Areas and Method of Manufacture Thereof," discloses an integrated circuit device.

Sincerely,

Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

OIPE
MAR 2 9 2004
PATENT & TRADEMARK

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
MSUN-98-002 CCC-CIPB	10/783,195
Applicant	
M.S. Lin et al.	
Filing Date	**Group Art Unit**
02/20/04	

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	5,212,403	5/18/93	Nakanishi et al.	257	664	9/6/91
	5,501,006	3/26/96	Gehman, Jr. et al.	29	840	5/9/94
	5,055,907	10/8/91	Jacobs	357	71	1/25/89
	5,635,767	6/3/97	Wenzel et al.	257	778	6/2/95
	5,106,461	4/21/92	Volfson et al.	205	125	12/21/90
	5,686,764	11/11/97	Fulcher	527	778	3/20/96
	5,083,187	1/21/92	Lamson et al.	357	71	4/16/91

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant